Washington State University
MAJOR CURRICULAR CHANGE FORM - - NEW/RESTORE COURSE

- ☐ **Please attach rationale for your request, a complete syllabus**, and explain how this impacts other units in Pullman and other campuses (if applicable).
- ☐ **Obtain all required signatures with dates.**
- ☐ **Provide original stapled packet of signed form/rationale statement/syllabus PLUS 10 stapled copies** of complete packet to the **Registrar's Office**, campus mail code 1035.
- ☐ **Submit one electronic copy of complete packet** to wsu.curriculum@wsu.edu.

Requested **Future** Effective Date: **Fall 2016** _____ (term/year) Course Typically Offered: **Fall** _____

DEADLINES: For fall term effective date: **October 1st**; for spring or summer term effective date: **February 1st**. See instructions.

NOTE: Items received after deadlines may be put to the back of the line or forwarded to the following year. Please submit on time.

☒ **New Course** ☐ Temporary Course ☐ **Restore Course**

ECE	543	Advanced Hardware Verification
course subject/crosslist	course no.	title

3 (3 _0_) **ECE 324**

Credit hrs	lecture hrs per week	lab or studio hrs per week	prerequisite

Description for catalog: Functional hardware verification for complex digital designs, including functional simulation, coverage metrics, event and assertion-based methods, property specification language, formal verification
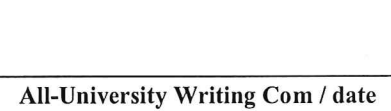
Additional Attributes: Check all that apply.

☐ Crosslisting (between WSU departments)*   ☐ Conjoint listing (400/500): _____

☐ Variable credit: _____   ☐ Repeat credit (cum. max. hrs): _____

Special Grading: ☐ S, F; ☐ A, S, F (PEACT only); ☐ S, M, F (VET MED only); ☐ H, S, F (PHARMACY, PHARDSCI only)

☐ Cooperative with UI   ☐ Other (please list request): _____

The following items require prior submission to other committees/depts. (SEE INSTRUCTIONS.)

☐ Request to meet Writing in the Major [M] requirement **(Must have All-University Writing Committee Approval.)**

☐ Request to meet UCORE in _____ **(Must have UCORE Committee Approval › › See instructions.)**

☐ Special Course Fee_____ **(Must submit request to University Receivables.)**

Contact: John Lynch _____ Phone number: (360) 546-9252 Campus mail code: VECS

Email: jdlynch@wsu.edu _____ Instructor, if different: _____

_____ 8/28/15 _____ 8/31/15 _____
Chair/date | **Dean/date** | **All-University Writing Com / date**

_____ | _____ | _____
Chair (if crosslisted/interdisciplinary)* | **Dean (if crosslisted/interdisciplinary)*** | **UCORE Committee Approval Date**

_____ | _____ | _____
Catalog Subcommittee Approval Date | **GSC or AAC Approval Date** | **Faculty Senate Approval Date**

***If the proposed change impacts or involves collaboration with other units, use the additional signature lines provided for each impacted unit and college.**

Rationale: 543 Advanced Hardware Verification

Verifying design correctness of increasingly complex system-on-chip designs poses a major challenge to the semiconductor industry. A study in 2002 by Collett International Research reports that 61% of first silicon tapeouts contain fatal flaws. And out of all tapeouts defective enough to require new masks, 60% contained functional or logic errors. These design defects can dramatically increase a project's overall cost and schedule. Design verification is consuming an ever-increasing portion of IC development time and cost. As much as 80% of effort in a complex IC design project is now devoted to verification

This course supports the proposed MSEE program's Lab-on-Chip (LoC) focus by teaching students the techniques necessary to verify design correctness of the digital subsystem of the LoC. The course is also useful for students studying digital system design outside of the LoC focus.

It does not affect other units in Pullman and other campuses.

ECE 543 Advanced Hardware Verification Course Syllabus

Description: Contemporary methods of functional hardware verification for complex digital designs, including functional simulation, coverage metrics, event and assertion-based verification, property specification language and formal verification techniques.

Credits: 3

Prerequisites by Topic:

1. An understanding of combinational and sequential digital system design
2. Working knowledge of Verilog hardware description language simulation

Required Texts:

Wile, Bruce; Goss, John, and Roesner, Wolfgang, *Comprehensive Functional Verification: The Complete Industry Cycle,* Morgan Kaufmann Publishers 2005, ISBN 0-12-751803-7

Foster, Harry, et al., *Assertion-Based Design, 2nd Edition*, Kluwer, 2003, ISBN 1-4020-8027-1.

Instructor: Dr. John Lynch

Office: VECS 301G
Phone: (360) 546-9252
Email: jdlynch@wsu.edu
Office hours: Whenever the office door is open
Lectures: MWF 10:10 – 11:00am, location TBA

Course Description

This course is application-oriented and covers practical aspects of functional hardware verification for complex ASIC and FPGA designs. It introduces the student to a variety of state-of-the art hardware design verification methods, including traditional functional simulation, assertion-based verification methodology and a subset of formal verification techniques. Topics covered include functional simulation, coverage metrics, testbench design and automation, event- and assertion-based verification, property specification language, and formal methods including model checking and logical equivalence checking.

In addition to lectures and reading, lab exercises will be assigned regularly throughout the course. Students will do functional simulation, assertion-based, and Property Specification Language (PSL) lab exercises using Mentor Graphics ModelSim digital simulation software

Course Procedures

There will be three hours of lecture each week. Reading from the required textbooks will be assigned each week. In addition to lectures and reading, four verification projects will be assigned regularly throughout the semester. Students will complete these projects using functional simulation, assertion-based, and Property Specification Language (PSL) lab exercises using Mentor Graphics ModelSim digital simulation software.

Attendance Policy

Lecture attendance is highly encouraged but not required. Students are nevertheless responsible for knowing any and all material presented in lecture.

Graduate Learning Outcomes (GLO)

GLO-1: Students will be able to utilize in-depth knowledge of digital hardware verification techniques to verify the design integrity of complex system-on-chip designs.

GLO-2: Students will be able to formulate and execute a system verification plan

GLO-3: Students will be able to present varication results through oral presentation and written reports

Learning Outcomes and Assessment

Student Learning Outcomes for this Course: At the end of the course, the students should be able to:	Course Topics/Dates: The following date(s) will address this outcome :	Evaluation of Outcome : This outcome will be primarily evaluated by:
Use functional simulation, coverage metrics, testbench design and automation to verify complex SoC designs	Primarily weeks 4-7, continuing throughout the course	CALC1, CALC2 and CALC3 verification projects
Use assertion-based verification methodology to verify complex SoC designs	Primarily weeks 8-11, continuing throughout the course	CALC2 and CALC3 verification projects
Students will be able to formulate and execute a verification plan	Weeks 2, 3	Verification plan
Students will be able to present varication results through oral presentation and written reports	Weeks 7, 11, 15	CALC1 and CALC2 written reports, CALC3 presentation and written report

Composition of final grade

The course grade will be determined by four verification project assignments as follows:

1. Verification plan	10%	
2. CALC1	30%	
3. CALC2	30%	
4. CALC3	30%	
Total	100%	

Grading Scale (% of total score)

A	93-100	B	83-86	C	73-76	D	60-66
A-	90-92	B-	80-82	C-	70-72	F	< 60
B+	87-89	C+	77-79	D+	67-69		

Rounding will be applied when calculating the grade.

Website

All course materials (lecture notes, assignments, etc.) will be available on the course Blackboard website at https://learn.wsu.edu/.

Make-up Exam/Assignment Policy

No make-up exams will be given, nor late homework assignment accepted, unless a medical or other emergency was the reason for missing the exam or the homework assignment. For any other reason you must first contact the instructor **before** missing an exam or an assignment.

Academic Integrity

Academic integrity is the cornerstone of the university and will be strongly enforced in this course. Any student found in violation of the academic integrity policy will be given an "**F**" for the course and will be referred to the Office of Student Conduct. For additional information about WSU's academic integrity policy/procedures, please contact (360) 546 9573.

Student with Disabilities

Reasonable accommodations are available for students with a documented disability. If you have a disability and need accommodations to fully participate in this class, please call the Access Center at (360) 546-9238 or van.access.center@wsu.edu. Accommodations may take some time to implement so it is critical that you contact the Access Center as soon as possible.

Emergency Notification System

WSU has made an emergency notification system available for faculty, students, and staff. Please register at zzusis with emergency contact information (cell, email, text, etc.). You may have been prompted to complete emergency contact information when registering for classes at RONet. In the event of a building evacuation, a map at each classroom entrance shows the evacuation point for each building. Please refer to it. Finally, in case of class cancellation campus-wide, please check local media, the WSU Vancouver web page and/or http://www.flashalert.net/. Individual class cancellations may be

made at the discretion of the instructor. Each individual is expected to make the best decision for their personal circumstances, taking safety into account. Safety plan website.

Audio, video, digital, commercial note-taking and other recording during class

Copyright 2015 John Lynch covers this syllabus, all lectures, and course-related written materials. During this course students are prohibited from making audio, video, digital, or other recordings during class, or selling notes to or being paid for taking notes by any person or commercial firm without the permission of the faculty member teaching this course.

ECE 543 Tentative Weekly Schedule

Week	Reading	Lecture Topics	Project Assignment
1	CFV Ch. 1	Course Overview, Introduction to verification	Write Verification Plan. Due Week 3 Friday.
2	CFV Ch. 2	Verification planning and flow	
3	CFV Ch. 3	Simulation-based verification; CALC1 project assignment	
4	CFV Ch. 4	Verification plan presentations	CALC1 verification project. Due Week 7 Friday.
5	CFV Ch. 5	HDL testbench architectures	
6	CFV Ch. 6	Verilog coding for testbenches Verification languages, verification coverage	
7	CFV Ch. 7; ABV Ch. 1, 2	Assertion-based verification; CALC2 project assignment	
8	CFV Ch. 8; ABV Ch 3	Intro. to Property Specification Language (PSL); CALC1 project solutions	CALC2 verification project (with assertions). Due Week 11 Friday.
9	CFV Ch. 9; ABV Ch 5, 6	CALC2 Q &A; PSL Sequences, temporal properties, and examples	
10	CFV Ch. 11; ABV Ch. 7, 8	Introduction to formal verification	
11	CFV Ch. 12	CALC3 project assignment	
12	CFV Ch. 13	Completing the verification cycle	CALC3 verification project. Present results during week 15.
13		CALC 3 Q & A.	
14	None	Work on project	
15		Presentation of CALC3 verification results	